Amendments to the Specification

Please replace the title with the following amended title:

OPERATIONAL AMPLIFIER HAVING LARGE OUTPUT CURRENT WITH LOW SUPPLY VOLTAGE

Kindly amend the specification as follows:

Page 1, between the title and the heading "**BACKGROUND OF THE INVENTION**", insert

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation application of application Serial No. 10/693,500 filed October 27, 2003, which is a continuation application of application Serial No. 10/392,080, filed March 20, 2003, now U.S. Patent No. 6,714,077, which is a continuation application of application Serial No. 10/017,928, filed December 18, 2001, now U.S. Patent No. 6,617,924, which is a continuation application of application Serial No. 09/574,109, filed May 19, 2000, now U.S. Patent No. 6,342,814, which are hereby incorporated by reference in their entirety for all purposes.--

Please replace the paragraph beginning on page 1, line 11 with the following amended paragraph:

The operational amplifier is composed of a differential input section 10 that

amplifies a differential voltage between two input signals inputted to an inverting or inverse input terminal 1 and to [[an]] a non-inverting or uninverse input terminal 2, an amplifying section 20Z that amplifies an output signal from the differential input section 10, an output section 30Z that outputs a signal amplified by the amplifying section 20Z to an output terminal 3 with a low output impedance, and a bias generating section 40 that generates a bias voltage necessary for the respective sections.

Please replace the paragraph beginning on page 3, line 20 with the following amended paragraph:

As shown in Fig. 3, if the voltage Vgs between the gate and the source of the n-channel MOS transistor 39 is held constant, it is necessary to widen the gate width W in order to obtain a large drain current Id. Also, it is apparent from the graph that the larger the voltage Vgs between the gate and the source is, the narrower the gate width W necessary for obtaining a given drain current Id [[isd]].

Please replace the paragraph beginning on page 6, line 21 with the following amended paragraph:

The operational amplifier is made up of a differential input section 10 that amplifies a differential voltage between two input signals inputted to an inverting or inverse input terminal 1 and to [[an]] a non-inverting or uninverse input terminal 2, an amplifying section 20 that amplifies an output signal from the differential input section

10, an output section 30 that outputs a signal amplified by the amplifying section 20 to an output terminal 3 with a low output impedance, a bias generating section 40 that generates a bias voltage necessary for the respective sections, and a step-up section 50 that steps up a supply voltage VDD to generate a step-up voltage VCP two to four times as large as the supply voltage VDD.

Please replace the paragraph beginning on page 7, line 27 with the following amended paragraph:

The output section 30 includes n-channel MOS transistors 31 and 32. A source of the n-channel MOS transistor 31 is ~~grounded~~ connected to the supply voltage VDD, a gate of the n-channel MOS transistor 31 is connected to the node N2, and a drain of the n-channel MOS transistor 31 is connected to the output terminal 3, respectively. A drain of the n-channel MOS transistor 32 is connected to the output terminal 3, a gate of the n-channel MOS transistor 32 is connected to the node N1, and a source of the n-channel MOS transistor 32 is grounded to the ground voltage GND, respectively.

Please replace the paragraph beginning on page 10, line 7 with the following amended paragraph:

Since the ~~supply~~ step-up voltage VCP (which is twice the supply voltage VDD or more) is supplied to the source of the p-channel MOS transistor 21, the signal V2 [[rises]] can rise to the supply voltage VDD or higher with a rise of the input differential

voltage Vin. For that reason, the voltage Vgs between the gate and the source of the n-channel MOS transistor 31 is increased, thereby allowing a larger drain current to flow through the n-channel MOS transistor in accordance with the characteristic shown in Fig. 3. The drain current that flows in the n-channel MOS transistor 31 is supplied to a load through the output terminal 3.

Please replace the paragraph beginning on page 15, line 25 with the following amended paragraph:

A drain of the p-channel MOS transistor 74b is connected to the node N1 that is connected with a gate of an n-channel MOS transistor 75. A ~~source~~ drain of the n-channel MOS transistor 75 is connected to the step-up voltage VCP, and a [[drain]] source of the n-channel MOS transistor 75 is connected to a gate of a p-channel MOS transistor 76 and also grounded to the ground voltage GND through an n-channel MOS transistor 77. A source of the p-channel MOS transistor 76 is connected to a drain of the p-channel MOS transistor 74a, and a drain of the p-channel MOS transistor 76 is connected to a drain and a gate of an n-channel MOS transistor 78 as well as a gate of an n-channel MOS transistor 79. A source of the n-channel MOS transistor 78 is grounded to the ground voltage GND. Also, a drain of the n-channel MOS transistor 79 is connected to the node N1, and a source of the n-channel MOS transistor 79 is grounded to the ground voltage GND. Other structures are identical with those in Fig. 2.

Please replace the paragraph beginning on page 18, line 5 with the following amended paragraph:

A drain of the n-channel MOS transistor 84b is connected to the node N1 that is connected with a gate of a p-channel MOS transistor 85. A ~~source~~ drain of the p-channel MOS transistor 85 is connected to the ground voltage GND, and a [[drain]] source of the p-channel MOS transistor 85 is connected to a gate of an n-channel MOS transistor 86 and also connected to the step-up voltage VCP through a p-channel MOS transistor 87. A source of the n-channel MOS transistor 86 is connected to a drain of the n-channel MOS transistor 84a, and a drain of the n-channel MOS transistor 86 is connected to a drain and a gate of a p-channel MOS transistor 88 as well as a gate of a p-channel MOS transistor 89. A source of the p-channel MOS transistor 88 is connected to the step-up voltage VCP. Also, a drain of the p-channel MOS transistor 89 is connected to the node N1, and a source of the p-channel MOS transistor 89 is connected to the step-up voltage VCP. Other structures are identical with those in Fig. 8.

Please replace the abstract with the following amended abstract:

An operational amplifier including ~~includes~~[[:]] a differential input section [[for]] generating a first signal as ~~corresponding to~~ a differential voltage between two input

signals; an amplifying section [[for]] amplifying the first signal ~~in voltage to generate~~ into second and third complementary signals; a first MOS transistor ~~connected~~ between a first supply voltage and an output node, a conduction state of the first MOS transistor [[being]] controlled responsive to ~~in accordance with~~ the second signal; a second MOS transistor ~~connected~~ between a second supply voltage and the output node, a conduction state of the second MOS transistor [[being]] controlled ~~in accordance with~~ responsive to the third signal; and a step-up section [[for]] stepping up the first and second supply voltages to generate a step-up voltage higher than the first and second supply voltages[[;]] ~~wherein,~~ the amplifying section [[is]] driven by the step-up voltage so that an absolute value of the maximum level of the second or third signal becomes larger than the absolute value of the first or second supply voltage.